inventors in U.S. Patent No. 5,430,864. Mr. Kenneth Olsen signed the declaration as an officer of the employer of the inventors (Sun Microsystems, Inc.). However, as noted in Applicants' response filed August 6, 1999, co-inventor Kong signed the declaration on behalf of all the inventors pursuant to Rule 1.63.

In the interests of expediting the prosecution, Applicants' preliminary amendment filed October 21, 1997 in Reissue Patent Application No. 5,430,864 is amended as required by the Examiner (Office Action dated 01/07/00, page 2) and is resubmitted herewith. Applicants respectfully seek reconsideration thereof.

I. Claims Rejected Under 35 U.S.C. § 251

The United States Patent and Trademark Office ("USPTO") has rejected claims 17-38 under 35 U.S.C. § 251 as being improper recapture of claimed subject matter deliberately canceled in the application for the patent upon which the present reissue is based. Applicants respectfully traverse this rejection.

The USPTO notes that the finally rejected and cancelled claims 55-72 fail to specify which bit of the stack pointer register is tested and do not have the setting (width indication bit) step. The USPTO asserts that deleting the setting step and/or reciting the least significant bit instead of the most significant bit is being tested amounts to recapture of the scope of cancelled claims 55-72 of the parent application *because* the combined scope of claims 1-38 can be interpreted as that the bit being tested can be set at *any bit position* within the stack pointer register. Applicants disagree and respectfully note that

"least significant bit" and "most significant bit" are technical computer science terms that an artisan would know refer to a *single bit position*. For example, "least significant bit" is "[t]he bit that carries the lowest value or weight in binary notation for a numeral; for example, when 13 is represented by binary 1101, the 1 at the right is the least significant bit." Sybil P. Parker, Editor in Chief, McGRAW-HILL DICTIONARY OF SCIENTIFIC AND TECHNICAL TERMS, Page 1063 (1989). Applicants note that claims 1-16 contain the limitation "most significant bit of the stack pointer register" and claims 17-38 contain the limitation "least significant bit of the stack pointer register." Therefore, the combined scope of claims 1-38 can **not** be interpreted as that the bit being tested can be set at *any bit position* within the stack pointer register, because only the (one single) "least significant bit" or "most significant bit" is tested, *i.e.*, not *any bit position* as the USPTO asserts. Applicants assert, therefore, that reciting the least significant bit instead of the most significant bit is being tested *does not* amount to recapture of the scope of cancelled claims 55-72 of the parent application because the combined scope of claims 1-38 can *not* be interpreted as that the bit being tested can be set at *any bit position* within the stack pointer register.

Applicants respectfully note that "[i]mpermissible recapture occurs in a reissue where the claims in the reissue are of the same scope as, or are broader in scope than, claims deliberately canceled in an application to obtain a patent. Where such claims also contain some narrowing limitation not present in the claims

deliberately canceled in the application, the Examiner must determine whether that narrowing limitation has a material aspect to it. If the narrowing limitation has a material aspect to it, then there is no recapture." Manual of Patent Examining Procedure (MPEP), 1412.03. Applicants note that claims 1-38 contain at least the above-mentioned material limitations not present in the claims deliberately canceled in the application for the patent upon which the present reissue is based. Therefore, there is no recapture. Accordingly, for the above-stated reasons, Applicants respectfully request the withdrawal of this rejection.

II. Claims Rejected Under 35 U.S.C. § 112, First Paragraph

The USPTO has rejected claims 17-38 under 35 U.S.C. § 112, first paragraph. Applicants respectfully traverse this rejection.

With respect to claims 17-38, the USPTO asserts that the specification, while being enabling for context switching by setting an indication at the most significant bit of a stack pointer register, does not reasonably provide for context switching by setting an indication at the least significant bit of a stack pointer register. Applicants disagree and respectfully direct the USPTO's attention to column 7, lines 37-47, of the instant specification. The above-referenced (second) paragraph in column 7 discloses that the most significant bit is important because it has the property that "it would not be expected to change at the low levels of addition or subtraction to be expected in address manipulations on the stack pointer," *i.e.*, as the stack pointer changes in value as frames are allocated and deallocated

on the stack, the high-order bit is not expected to change. However, an artisan would realize that the most significant bit is not the only bit with that property (notwithstanding the first sentence of the referenced paragraph) because, as disclosed at column 8, lines 40-44, stack frames on SPARC, as on many other architectures, must be "aligned on four byte boundaries." An artisan would realize that this means that the *least significant bit* also does not change in value as stack frames are allocated and deallocated. Therefore, a person skilled in the art would realize that this allows the *least significant bit* to be used as the indicator that the stack pointer points to a 64-bit frame instead of a 32-bit frame. Pointers to 32-bit frames would keep the low-order bit zero. Pointers to 64-bit frames would have one the low-order bit set to one. References to the objects on the 64-bit stack frame would use appropriate address arithmetic when using the stack pointer directly to account for the presence of this bit. This has the further advantage that a reference made incorrectly (*e.g.*, assuming a 64-bit stack pointer when it is really a 32-bit stack pointer, or vice versa) will result in an alignment exception, allowing incorrectly executing programs to be caught and terminated. Accordingly, for the above-stated reasons, Applicants submit that its specification does reasonably provide enablement for context switching by setting an indication at the *least significant bit* of a stack pointer register.

In view of the foregoing, Applicants respectfully request

that the rejection of claims 17-38 under 35 U.S.C. § 112, first paragraph, be withdrawn.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance, and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: April 7, 2000

Eric S. Hyman
Reg. No. 30,139

Enclosure

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box AF, Assistant Commissioner for Patents, Washington, D.C. 20231, on April 7, 2000.

Azar Burnham April 7, 2000